

Commodore

A 500 PLUS

**INCLUDES A 501 PLUS
RAM EXPANDER**

Service Manual

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PN-400420-01



Commodore

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SERVICE MANUAL

**A500 PLUS
INCLUDES A501 PLUS
RAM EXPANDER**

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PN-400420-01

INTERNATIONAL EDITION

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SECTION 1
SPECIFICATIONS

A500 PLUS

A500 PLUS SPECIFICATIONS

INTRODUCTION

The A500 Plus is a feature enhanced version of the A500 personal computer.

FEATURES

CPU: 7.16 MHz 68000 NTSC; 7.09 MHz 68000 PAL

Memory: 1 Megabyte standard expandable to 2 MB with addition of A501 Plus

Kickstart ROM: 512K (V2.04)

Mass Storage Memory: Internal, 3.5 inch FDD mounted on the right side, the same as the A500.

Additional Features: Real Time Clock (on-board) with battery backup.

APPEARANCE

The A500 Plus appearance shall be the same as the A500. A new logo plate has been added to distinguish "A500" from "A500 Plus". The color is the same light beige as the current A500.

WHAT'S ADDED

1 Meg on-board memory expandable to 2 Meg.

8375 FAT AGNUS which supports 2 Meg. of Chip RAM

On-board Real Time Clock

8373 ECS Denise

Full ECS support

V2.04 in ROM

CUSTOM CHIPS

The A500 Plus shall contain the same custom chip set as the A500, except for the 8375 2Meg. FAT AGNUS and 8373 ECS Denise.

SYSTEM I/O

EXTERNAL SYSTEM I/O

External floppy, Serial, Parallel, Mouse, Joystick, Stereo Audio Ports

These Ports remain unchanged from their A500 counterparts.

MEMORY MAP

The A500 Plus Memory Map is the same as the A500 Memory Map.

A501 PLUS

A501 PLUS SPECIFICATIONS

DESCRIPTION

The A501 Plus is a memory expansion board for the Amiga 500 Plus personal computer. It has 1 MB of "chip" memory and interfaces directly to the A500 Plus memory expansion slot. Unlike the A501, the A501 Plus doesn't have a Real Time Clock (RTC), the A500 Plus has a built-in RTC.

The A501 can be used in either the A500 or A500 Plus personal computer, has 512K of memory and includes a Real Time Clock. The A500 maps the A501 into pseudo-fast memory while the A500 Plus maps it into chip memory. In addition, when used in an A500 Plus system, the internal (built-in) RTC is selected.

Both the A501 and A501 Plus uses the same printed circuit board (PCB). In the A501 Plus, the RTC and refresh feature components are not loaded.

MEMORY TYPE

The A501 Plus shall use 256K x 4 120ns DRAMs.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
+5	1-2, 51-52	I	+ 5 Volts
GND	3-4, 21-22, 53-54		Signal Ground
XDRD (0-15)	5-20	I/O	Memory Data Bus
XDRA (0-8)	23-31	I	Memory Address Bus
/EXTICK	32	O	Active low. When this signal is asserted, it allows the A500 to detect the presence of an A501. The A501 Plus does not use this signal.
/XCLKS	33	I	Active low. When this signal is asserted, the external RTC is selected. This signal is not used in the A501 Plus.
/XOE	34	I	Active low. When this signal is asserted, data can be read from the expansion memory.
/XCASL	35	I	Active low. This signal strobes the column address into DRAMs and corresponds to the low byte of the data word.
/XCASU	36	I	Active low. This signal strobes the column address into the DRAMs and corresponds to the high byte of the data word.
/XRAS1	37	I	Active low. This signal strobes the row address into the DRAMs and corresponds to the upper 512K of the expansion RAM.
/XRAS0	38	I	Active low. This signal strobes the row address into the DRAMs and corresponds to the lower 512K of the expansion RAM.
/XWE	39	I	Active low. When this signal is asserted, data is written into the expansion memory.
NC	40, 56		Not connected.
XD (0-3)	41-44	I/O	RTC Data bus. These lines are not used in the A501 Plus.
XA (2-5)	45-48	I	RTC Address Bus. These lines are not used in the A501 Plus.
/XCLKRD	49	I	Active low. When this signal is asserted, data can be read from the RTC. This signal is not used in the A501 Plus.
/XCLKWR	50	I	Active low. This signal strobes the data and address into the RTC. This signal is not used in the A501 Plus.
+12V	55	I	+ 12 Volts. This is used on the A501 to charge the battery. This line is not used on the A501 Plus.

A501 PLUS SPECIFICATIONS (Continued)

FACTORY DEFAULT JUMPER SETTINGS

	JP1	JP2A	JP2B	JP3	JP9
A501	1-2 shorted	1-2 open 2-3 shorted	1-2 open 2-3 shorted	1-2 shorted 1-2 shorted 1-1 open 2-2 open	1-2 open
A501 Plus	1-2 shorted	1-2 shorted 2-3 open	1-2 shorted 2-3 open	1-2 shorted 1-2 shorted 1-1 open 2-2 open	1-2 open

Jumper Function

- JP1** When 1-2 are shorted, /EXTICK detection is enabled. This jumper has no effect on the A501 Plus, because it does not use /EXTICK detection.
- JP2A, JP2B** When 2-3 are shorted (1-2 open), it enables the refresh feature in the A501. Refresh components U11-U13 must be loaded in the A501. The refresh feature is only required on the A501 to compensate for refresh deficiencies in older revs of the A500.
- JP3** Swaps upper and lower bank DRAMs. When 1-2 are shorted (1-1 and 2-2 open), /XRAS0 and /XRAS1 selects the lower and upper banks respectively. Conversely, when 1-1 and 2-2 are shorted, /XRAS0 selects the upper bank while /XRAS1 selects the lower bank RAMs.
- JP9** Overwrites /XCLKS. When 1-2 are shorted, /XCLKS is permanently enabled and the A501 (external) RTC is always selected. This jumper is normally open. Selection of internal or external RTC is done by the A500 or A500 Plus via the /XCLKS line. RTC components U9, U11-U13, C9, C11-C13, C911, C913, R911-R915, D11-D9123, BT9, TC9 and Y9 must be loaded in the A501.

DIMENSIONS

- Length: 5.5 in.
- Width: 3.5 in.

POWER

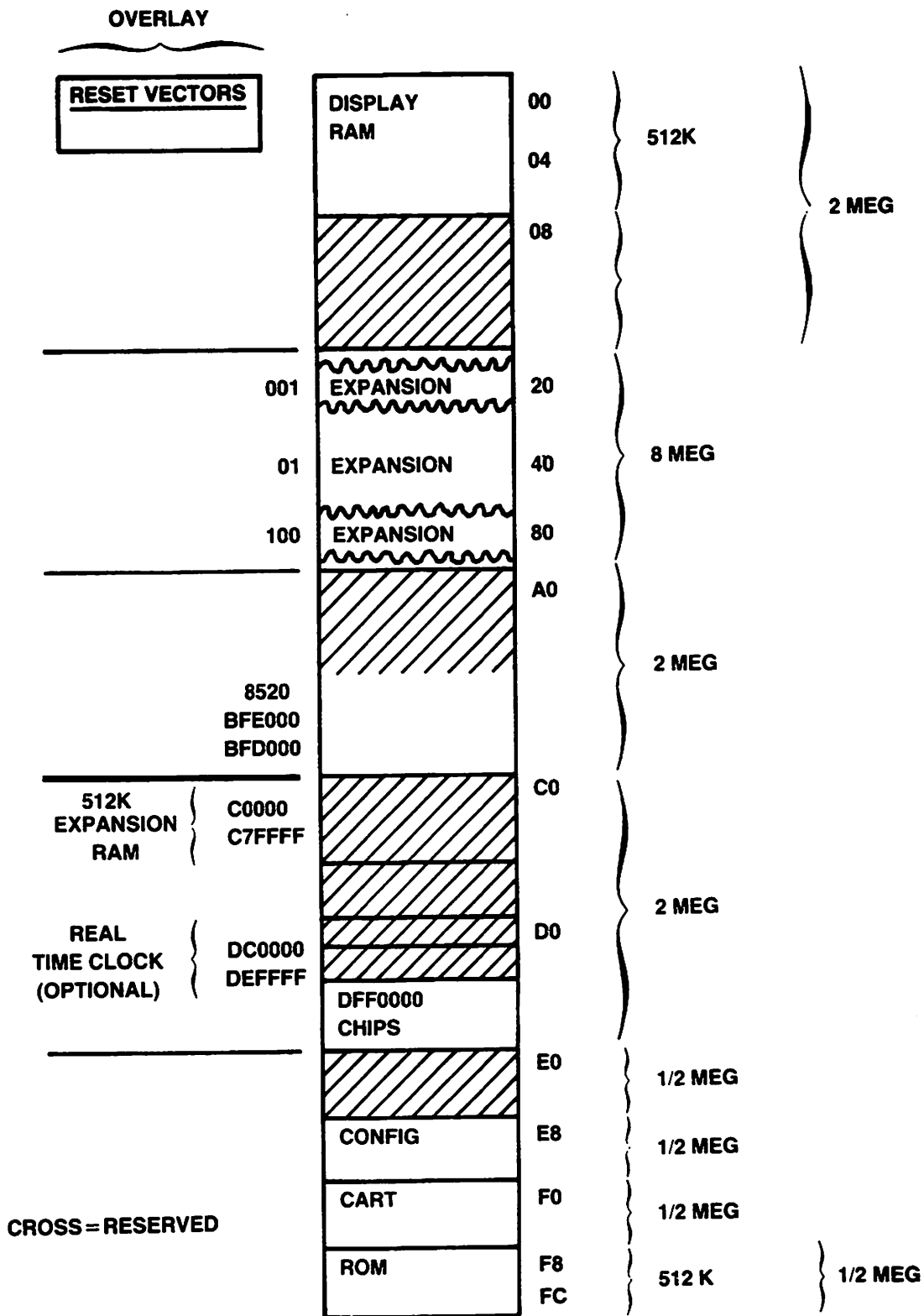
- +5VDC @330 mA MAX for A501 Plus
@280 mA MAX for A501
- +12VDC @15 mA MAX for A501
Not Used on A501 Plus

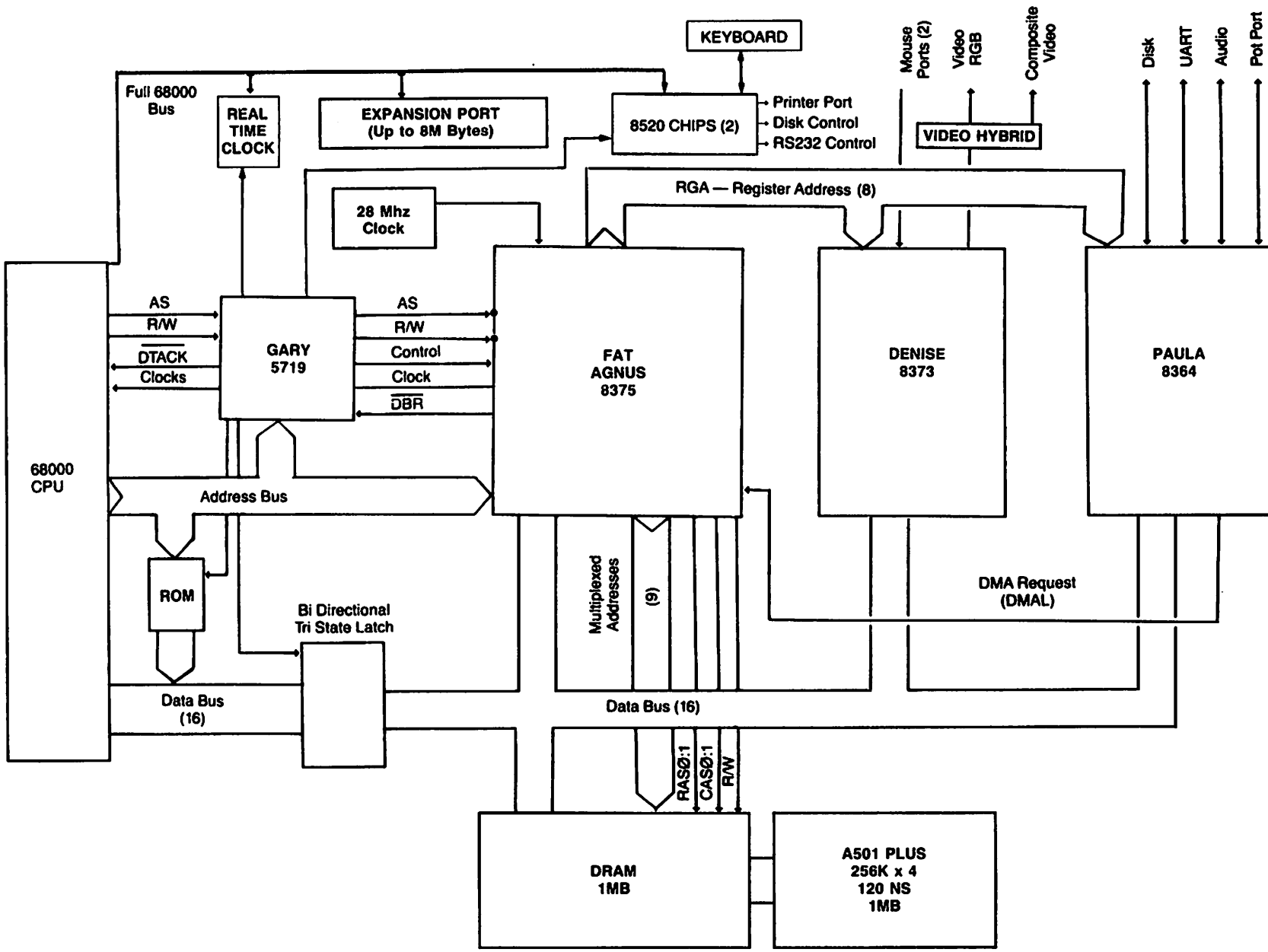
ENVIRONMENT

- Operating Temperature 0 to +55°C
- Humidity Up to 90% without condensation

SECTION 2
THEORY OF OPERATIONS

AMIGA 500 PLUS MEMORY MAP





A500 PLUS BLOCK DIAGRAM

A500 PLUS SERVICE MANUAL

THEORY OF OPERATION

The AMIGA 500 Plus computer is a high-performance system with advanced graphics and audio features. The principal hardware features consist of the 68000 microprocessor which runs at 7.2 MHz, 1MB RAM, expandable to 2MB, and configurable to 8MB, 2 parallel I/O chips, one control chip (GARY) and 3 custom VLSI chips that provide the unique capabilities for animation, graphics and sound.

68000 MICROPROCESSOR

The 68000 is the CPU of the system. All other resources are under software control via control data issued from it. All 3 custom chips have control registers that are written by the 68000.

The 68000 communicates with the rest of the computer via its address bus, data bus and control lines. Notice that in the block diagram the 3 custom chips do not reside directly on the 68000 buses. When the 68000 starts a bus cycle that is intended for the custom chips or the display RAM, the bus control chip detects whether or not the display RAM buses are available. The control chip will not assert the acknowledge signal (/DTACK) back to the 68000 until the display RAM buses are available. Once the 68000 receives /DTACK it completes the bus cycle. Connecting the display RAM buses to the 68000 buses is discussed further in the section on bus control. Because the display RAM is capable of approximately twice the bandwidth of the 68000, the 68000 is usually not delayed by waiting for the display buses to become available.

The 68000 can fetch instructions from:

- Display RAM
- ROM

The 68000 can read and write data directly to:

- Display RAM
- Parallel I/O Chips
- 3 Custom I.C.s
- ROM

The 68000 transmits data and control to and from the peripherals via the parallel I/O and the 3 custom chips.

7M is the processor clock to the 68000. C1, C3 and CDAC are used to clock the custom chips and determine the timing of signals to the memory arrays.

ROM

The ROM contains the kernel and DOS routines; it is 128K × 16.

PARALLEL I/O

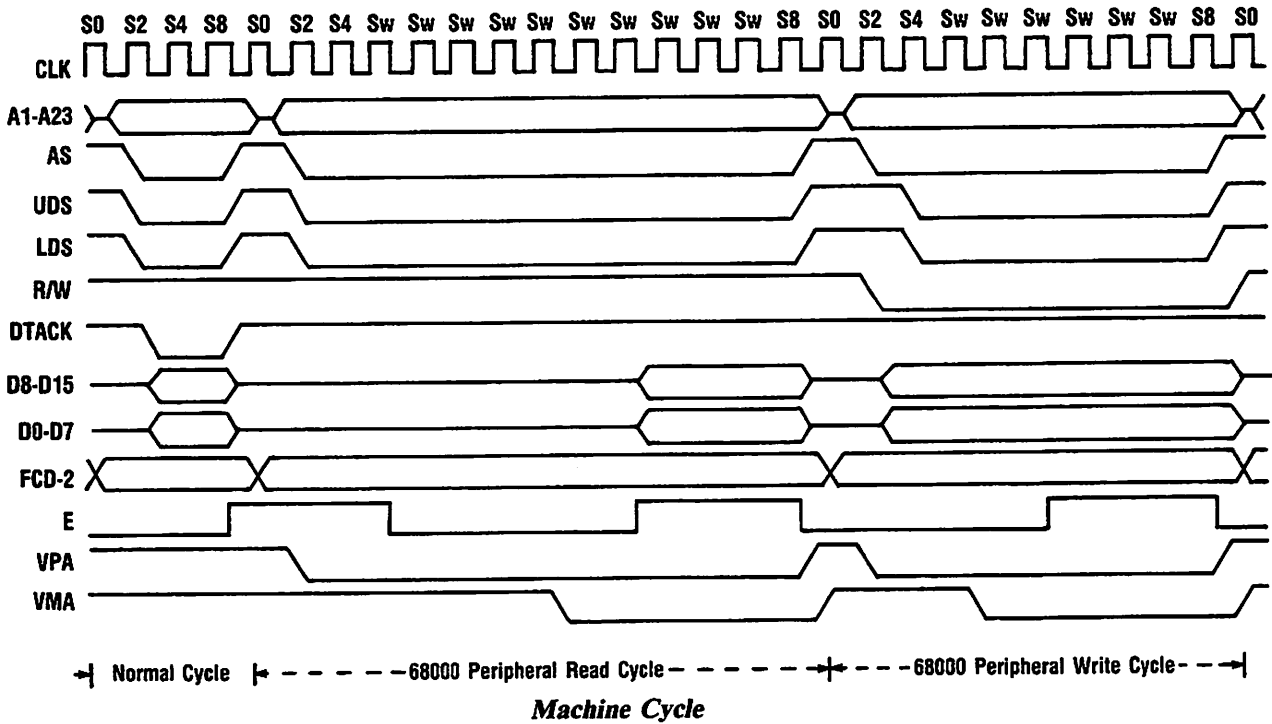
The 2 multipurpose 8520 I/O chips provide the following:

- I/O to and from the parallel port connector
- Control lines to and from the joystick/mouse ports
- A control line to the front panel LED
- Internal control lines
- Keyboard control lines, clock and data
- Serial port control lines
- Floppy disk interface control lines
- Internal timers

These 2 chips reside on the 68000 buses and are read and written by the 68000.

THEORY OF OPERATION (Continued)

CPU SIGNAL SUMMARY



Signal Name	Mnemonic	Input/Output	Active State	Three State
Address Bus	A1-A23	Output	High	Yes
Data Bus	D0-D15	Input/Output	High	Yes
Address Strobe	\overline{AS}	Output	Low	Yes
Read/Write	R/\overline{W}	Output	Read-High Write-Low	Yes
Upper and Lower Data Strobes	$\overline{UDS}, \overline{LDS}$	Output	Low	Yes
Data Transfer Acknowledge	\overline{DTACK}	Input	Low	No
Bus Request	\overline{BR}	Input	Low	No
Bus Grant	\overline{BG}	Output	Low	No
Bus Grant Acknowledge	\overline{BGACK}	Input	Low	No
Interrupt Priority Level	$\overline{IPL0}, \overline{IPL1}, \overline{IPL2}$	Input	Low	No
Bus Error	\overline{BERR}	Input	Low	No
Reset	\overline{RESET}	Input/Output	Low	No*
Halt	\overline{HALT}	Input/Output	Low	No*
Enable	E	Output	High	No
Valid Memory Address	\overline{VMA}	Output	Low	Yes
Valid Peripheral Address	\overline{VPA}	Input	Low	No
Function Code Output	FC0, FC1, FC2	Output	High	Yes
Clock	CLK	Input	High	No
Power Input	Vcc	Input	—	—
Ground	GND	Input	—	—

*Open Drain
A0 is internal to 68000

THEORY OF OPERATION (Continued)

CLOCKS GENERATOR

The entire computer board is run synchronously to the 3.57954Mhz color clock (C1). This is accomplished by generating a number of sub-multiple frequencies from our master 28.63636Mhz crystal oscillator. The following are the primary clocks on the board:

Name	Description
C1	The 3.579545Mhz Color Clock
C2	C1 shifted 45 degrees later
C3	C1 shifted 90 degrees later
C4	C1 shifted 135 degrees later
7M	C1 XORed with C3* (7.15909Mhz)
DAC	7M shifted 90 degrees later

7M is the processor clock for the 68000 microprocessor. C1-C4 and DAC are used to clock the custom chips and for determining the timing of signals to the memory arrays.

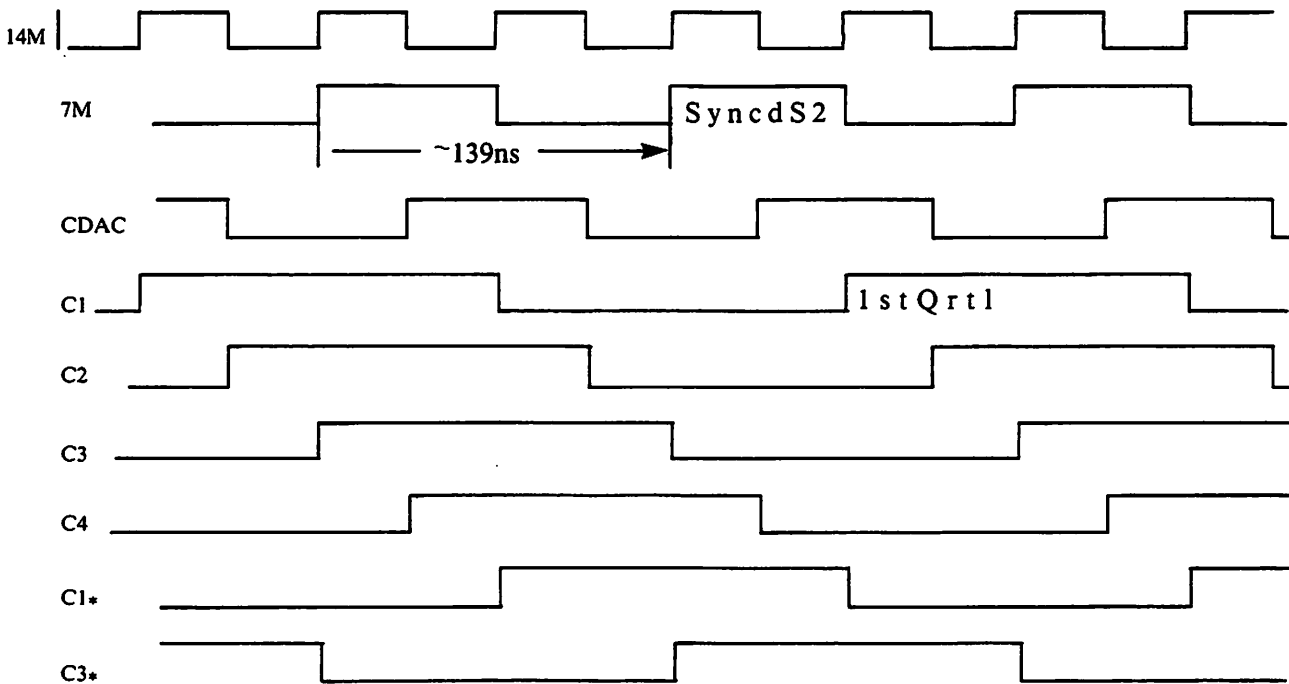
The above frequencies are true for NTSC Amigas. A PAL Amiga will operate slightly slower, with a main clock of 28.37516Mhz. This is divided down to get 7M = 7.09379Mhz and C1 = 3.546895Mhz. A special circuit is required to take five fourths of C1 to derive the PAL colorburst frequency of 4.43361875Mhz.

The following clocks are available at the edge connector:

Name	Pin	Description
C3*	14	C3 inverted
CDAC	15	DAC equivalent
C1*	16	C1 inverted

Note that 7M (the processor clock) is not available at the connector; it can be easily generated by:
 $C3^* \text{ XNOR } C1^* = 7M \text{ equivalent}$

If you need a 14.31818Mhz synchronous clock, you can generate it by:
 $(7M_{equiv}) \text{ XOR } (CDAC) = 14M \text{ equivalent}$



Amiga System Clocks

THEORY OF OPERATION (Continued)

THE 3 CUSTOM CHIPS

The 3 custom chips provide very fast manipulation of graphics and audio data in the display RAM. All the major functions in the chips are DMA driven; that is, streams of data are moved between the custom chips and display RAM under DMA control. These streams of data are acted upon by the custom chips. Fat Agnus, custom chip #1, contains 25 dedicated purpose DMA counters.

The 3 chips have control registers which are usually loaded by the 68000. However, Fat Agnus also has the capability of loading control registers in the other 2 custom chips. When Fat Agnus performs a bus cycle, it outputs a code on the Register Address Bus telling the other 2 chips the nature of the bus cycle. This is necessary because many of the bus cycles provide data to or from the other 2 chips, thus they must cooperate appropriately.

In addition to manipulating data in the display RAM, the custom chips output streams of data to the video output circuits and audio output circuits, and they move data to and from the floppy disks and serial port.

Note that the display RAM buses can be completely isolated from the 68000 buses by Fat Agnus and Data Bus drivers. Thus, Fat Agnus can be performing a bus cycle on the display buses simultaneously with the 68000 performing a bus cycle on its buses. This parallelism increases throughout.

BUS CONTROL, ADDRESS/DATA MUX, ADDRESS DRIVER

The bus control logic resides in the control chip (GARY) and Fat Agnus. They provide 3 major functions, they:

Synchronize the 68000 to the current phase of C1

Arbitrate between the 68000 and Fat Agnus for the display buses

Generate DRAM timing for the video RAM bus drivers appropriate to the current cycle

Synchronizing the 68000 to C1 is straightforward, since the 68000 is clocked by 7M which is twice the frequency and synchronous to C1. If the 68000 starts a bus cycle in the wrong phase of C1, the bus control chip merely delays /DTACK long enough so that the 68000 will complete the bus cycle in the desired phase relationship to C1. This phase relationship is necessary because the custom chips and the display RAM are clocked by C1.

Arbitration is very simple. Fat Agnus tells the bus control prior to taking the display RAM buses by asserting an input to the control chip (GARY) called /DBR. Whenever Fat Agnus has the display buses and the 68000 wants them, the 68000 is held off by not giving it /DTACK. In this state the 68000 has no effect on the display buses until the bus controller enables the bus drivers.

Fat Agnus generates the DRAM timings and does all address multiplexing. If the 68000 is running a video memory cycle, its addresses are routed through Fat Agnus onto the multiplexed address lines. If the custom chips are running a memory cycle the addresses are routed to the multiplexed address lines from internal address register.

DISPLAY RAM

The display RAM is a 512K read/write memory that resides on the RAM address and RAM data buses. It is expandable to 1M bytes by the addition of the RAM expansion module. It is implemented using standard 256K x 1 dynamic RAMs, refreshed by Fat Agnus.

The display RAM is really used for much more than just holding graphics data. It also stores code and data for the 68000.

CUSTOM CONTROL CHIPS

The Amiga's animation, graphics and sound are produced by three custom chips. Fat Agnus (8375), High Res Denise (8373) and Paula (8364). A fourth custom chip, Gary serves as the control chip. The following pages include feature lists, and block diagrams for these chips.

8375 AGNUS (Continued)

BITPLANE ADDRESSING

Some computer bitmap displays are organized so that the bitplanes for each pixel are all located within the same address. This is called pixel addressing. If the entire data word of one address is used for a single pixel with 8 bit planes, the data word will look like this. (numbers are bitplanes): 12345678-----

The data compression can be improved by packing more than one pixel into a single address like this: 1234567812345678 or like this, if there are only 4 bitplanes: 1234123412341234

The IC device, uses a bitmap technique called Bitplane Addressing. This separates the bitplanes in memory. To create a 4 plane (16 color) image, the bitplane display DMA channels fetch from 4 separate areas of memory like this:

```
1111111111111111
2222222222222222
3333333333333333
4444444444444444
```

These are held in buffer register and are used together as pixels, one bit at a time, by the display (left to right).

This technique allows reduced odd numbers of bitplanes (such as 3 or 5) while maintaining packing efficiency and speed. It also allows grouping bitplanes into 2 separate images, each with independent hardware high speed image manipulation, line draw, and area fill.

DMA CHANNEL FUNCTIONS

Each channel has an 20 bit RAM address pointer that is placed on the MA memory address bus, and is used to select the location of the DMA data transfer from anywhere in 1M words (2M bytes) of RAM.

An eight (8) bit destination address is simultaneously placed on the register address bus (RGA), sending the data to the corresponding register.

In a typical DMA channel, almost all channels have DRAM as source and chip registers as destination.

The pointer must be preloaded and is automatically incremented each time a data transfer occurs.

Each controller utilizes one or more of these DMA channels for its own purposes. The following is a brief summary of these controllers and the DMA channels they use.

A-Blitter (four (4) channels)

The Blitter uses four (4) DMA channels, Three source and one (1) destination as previously described.

Once the Blitter has been started, the four (4) DMA channels are synchronized and pipelined to automatically handle the data transfers without further processor intervention. The images manipulated in memory, independent of the display (bitplane DMA).

B-Bitplane (six (6) channels)

The bitplane controller continuously (during display) transfers display data from memory to display buffer registers. There are six (6) DMA channels to handle the data from six (6) independent bit planes. The buffers convert this bitplane data into pixel data for the display.

C-Copper (one (1) channel)

The Copper is a co-processor that uses one of the DMA channels to fetch its instructions. The DMA pointer is the instruction counter and must be preloaded with the starting address of the Copper's instructions.

The Copper can move (write) data into chip registers. It can skip, jump, and wait (halt). These simple instructions give great power and flexibility because of the following features.

When Copper is halted, it is off the data bus, using no bus cycles until the wait is over. The programmed wait value is compared to a counter that keeps track of the TV beam position (beam counter) and when they are equal, the Copper will resume fetching instructions.

It can cause interrupts, reload the color registers, start the Blitter or service the audio. It can modify almost any register inside or outside the IC device, based on the TV screen coordinates given by the Beam Counter and the actual address encoded on the RGA Bus.

8375 AGNUS (Continued)***DMA CHANNEL FUNCTIONS (Continued)******D-Audio (four (4) channels)***

There are four (4) audio channels, all of which are located outside of the audio DMA Controller section of Agnus. Each controller is independent and uses one DMA channel from the DMA Controller and fetches its data during a dedicated timing slot within horizontal blanking. This is accomplished by a controller asserting the DMAL input on the DMA Controller.

E-Sprites (eight (8) channels)

There are eight (8) independent Sprite controllers, each with its own DMA channel and its own dedicated time slot for DMA data transfer. Sprites are line buffered objects that can move very fast because their positions are controlled hardware registers and comparators.

Each sprite has two (2) sixteen bit data registers that define a 16 pixel wide Sprite with 4 colors. Each has a horizontal position register, a vertical start position register and a vertical stop position register. This allows variable vertical size sprites.

The Sprite DMA controller fetches image and position data automatically from anywhere in 2 Megabytes of memory depending on device pin configuration.

Sprites can be run automatically in DMA mode or they can be loaded and controlled by the microprocessor.

Each Sprite can be re-used vertically as often as desired. Horizontal re-using is also allowed with microprocessor control.

F-Disk (one (1) channel)

The disk controller, which is located outside of the DMA, uses a single DMA channel from the device. The controller uses the DMA time slot for data transfer and can read or write a block of data up to 128K anywhere in 2 Megabytes of memory depending on device pin configuration.

G-Memory Refresh (one (1) channel)

The refresh controller uses a single DMA channel with its own time slots. It places RAS addresses on the memory address bus (MA) during these slots, in order to refresh the dynamic RAM. Memory is refreshed on every raster line.

During the DMA no data transfer actually takes place. The register address bus (RGA) is used to supply video synchronizing codes. At this time RAS1* and RAS are low. CASU* and CASL* are inactive during this cycle.

RAM AND REGISTER ADDRESSING

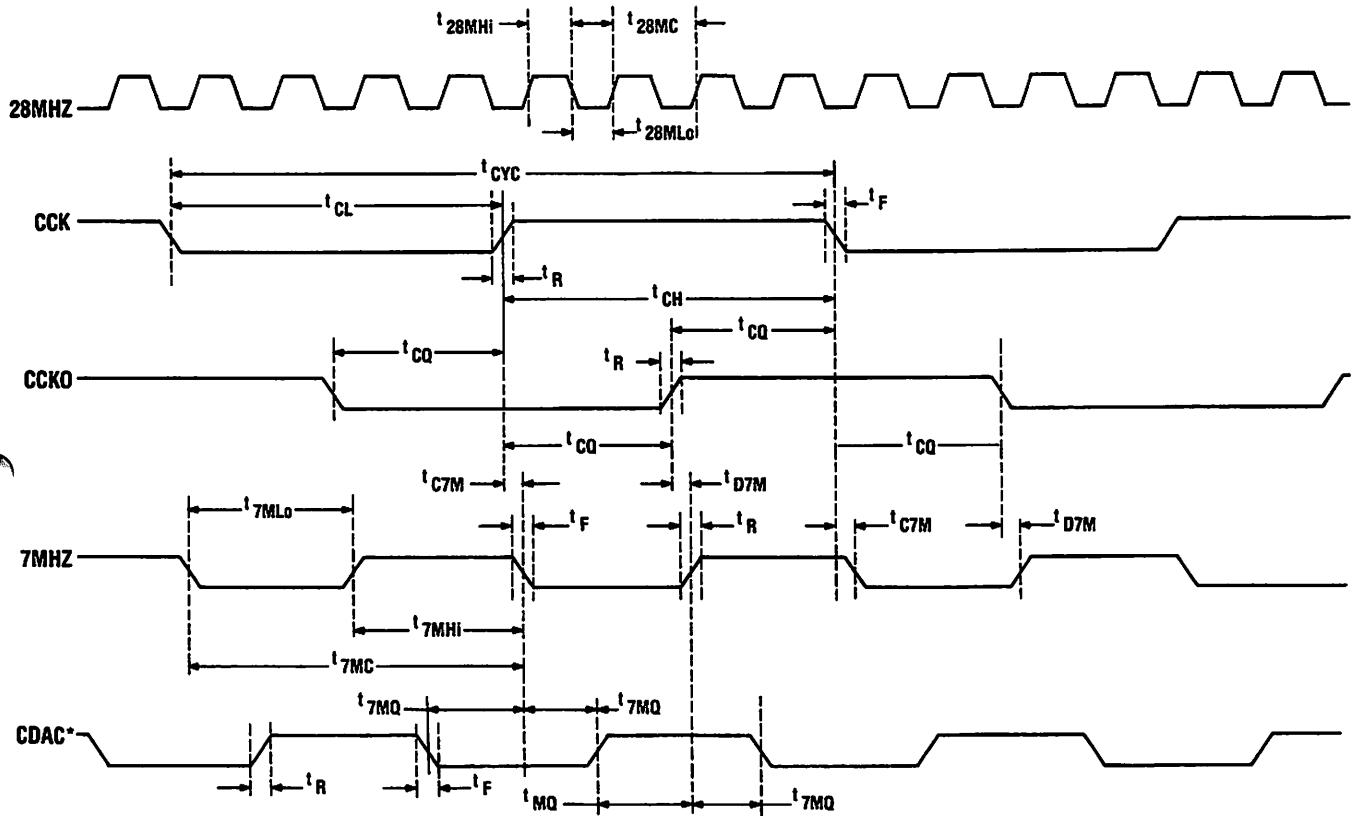
The device generates RAM addresses from two sources, the processor or the device performing DMA cycles. The processor accesses RAM whenever AS* and RAMEN* are both low. At this time, the device also multiplexes the processor address (A1-A20) onto the MA bus. During row address time A9-A17 and A19 are placed onto MA0-MA8, MA9, respectively; during column address time A1-A8, A18 and A20 are placed onto MA0-MA7, MA8 and MA9, respectively. In the 1 meg configuration, A19 is still used to determine the RAS line to be asserted. If A19 is low RAS0* is active and if high RAS1* is active. In the 2 meg option RAS will always be active on a RAM access. The IC will assert CASL* if LDS* is low or CASU* if UDS* is low.

When the device needs to do a DMA cycle, the device disables the processor from accessing RAM by asserting the Data Bus Request Line (DBR*). At this time, the device multiplexes its generated RAM address onto the MA lines and will activate RAS and the proper RAS0* or RAS1* line unless it is a refresh cycle where all RAS lines are active. During a DMA cycle, the IC device will also assert both CASU* and CASL*, unless it is a refresh cycle where they both remain inactive.

The device also generates RGA addresses from either the processor or device DMAs, each of which is selected by an internal multiplexer. This multiplexer allows the processor to perform a register read/write access when AS* and RGEN* are both low. The device then takes the low order byte of the processor address A1 to A8 and reflects its value on the RGA output bus RGA1 to RGA8. The device will reflect the status of PRW input on the RRW output line, to indicate a memory read or write operation.

During a device DMA cycle, the device prevents the processor from doing a register access by asserting the DBR* line. The device will then place the contents of its register address encoder onto the RGA bus.

8375 AGNUS (Continued)



Clock Relations

CLOCK RELATIONS (Refer to Figure above)

	SYMBOL	MIN	MAX	UNIT
2.4.1 28MHz clock cycle	t_{28MC}	34.57		ns
2.4.2 28MHz clock high	t_{28MHi}	12.0	22.9	ns
2.4.3 28MHz clock low	t_{28MLo}	12.0	22.9	ns
2.4.4 CCK clock cycle	t_{CYC}	260	290	ns
2.4.5 CCK clock high	t_{CH}	130	150	ns
2.4.6 CCK clock low	t_{CL}	130	150	ns
2.4.7 CCK-CCKQ clock separation	t_{CQ}	65	75	ns
2.4.8 7MHz clock cycle	t_{7MC}	130	150	ns
2.4.9 7MHz clock high	t_{7MHi}	65	75	ns
2.4.10 7MHz clock low	t_{7MLo}	65	75	ns
2.4.11 7MHz-CDACQ clock separation	t_{7MQ}	30	40	ns
2.4.12 CCK to 7MHz delay	t_{C7M}	0	15	ns
2.4.13 CCKQ to 7MHz delay	t_{Q7M}	0	15	ns
2.4.14 Clock rise time	t_R	0	10	ns
2.4.15 Clock fall time	t_F	0	10	ns

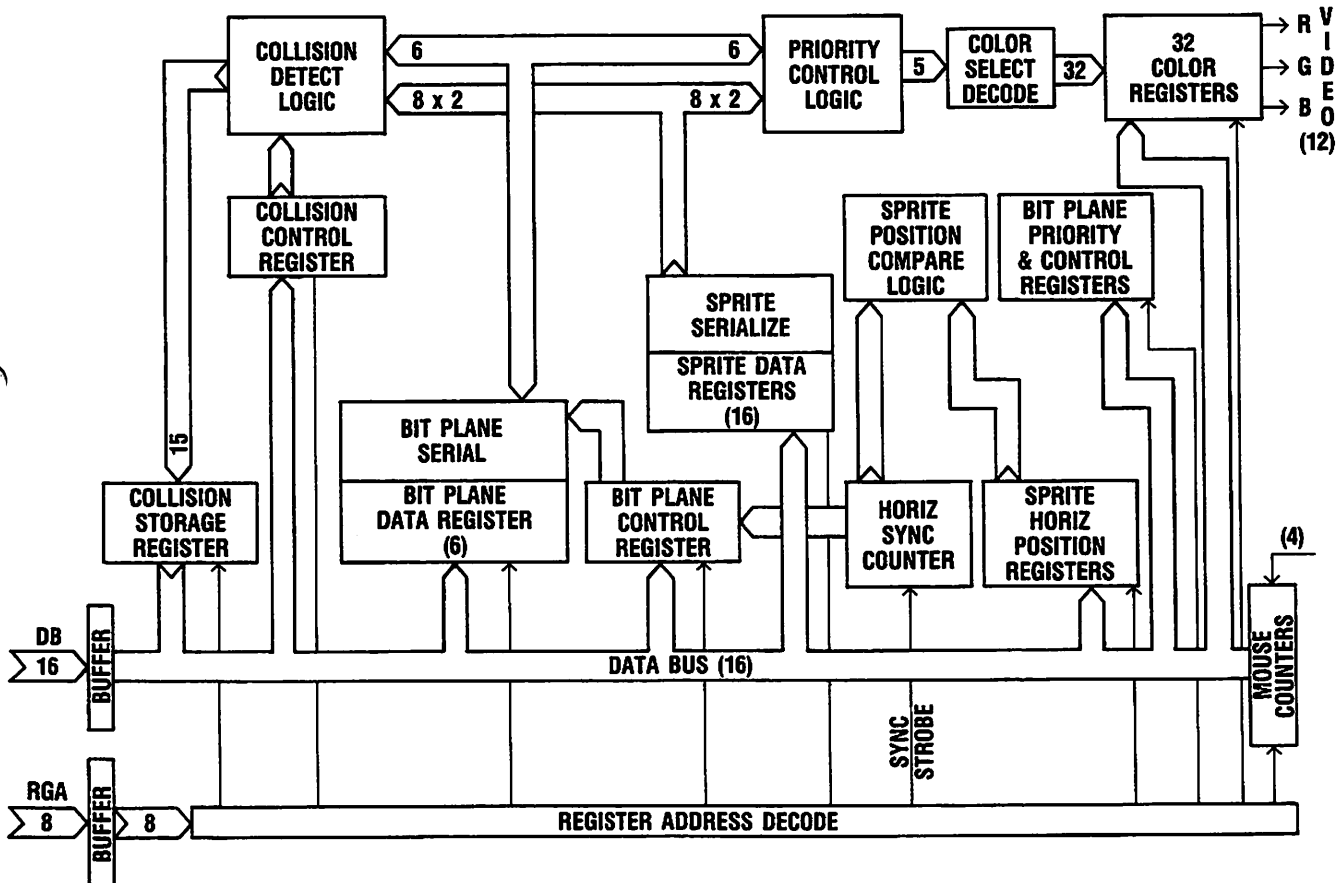
8373 DENISE HI RES

MAIN FUNCTIONS

- Display data buffer, encode display object to RGB colors.
- Bitplane & Sprite display. Parallel data from data bus is retained in six (6) Bitplane and eight pairs of Sprite data buffers.
- Bitplane Data loaded and serialized during display activity.
- Sprite Data loaded during display inactivity — individual serialization occurs when Sprite position Compare logic detects equality between the Sync Counter and any Sprite Position Register.
- Six (6) lines of Bitplane & eight (8) pairs of serial data go to Priority control logic which selects only one (1) of the Sprites or one (1) of the separate Bitmap images to produce the five (5) bit color select code at its output. This five (5) bit code then selects one of the thirty-two (32) color registers to produce the twelve (12) bit RGB video output.
- The Bitplane and Sprite serial lines also go to the Collision Detect Logic, which detects real time coincidence between them, and sets appropriate bits in the Collision Storage register. This register is read and cleared by the 68000.
- The four (4) "mouse counters" are controlled by the two (2) mouse-joystick connectors. These count the pulses representing the horizontal and vertical motion of two (2) "mouse" controllers, and are read by the 68000.

CHIP ELEMENTS

32 Color Registers; Bitplane Priority and Control Registers; Color Select Decoder; Priority Control Logic; 16 Sprite Serial Lines; Sprite Data Registers; Bit Plane Control Registers; Two (2) Mouse Connectors; Sprite Position Compare Logic; Sprite Horizontal Control Registers; Bit Plane Serializer Collision Detect Logic; Collision Control Register; Collision Storage Register; Buffer — Data Bus; Buffer — Register Address Decode; Bit Plane Data Registers Video: RGB; Sprite Serialization.



Denise Block Diagram

8364 PAULA

Paula is the Port, Audio and Uart chip. Its main function is the four audio channels. It also contains the I/O ports, (Disk and Pots), Serial Port (Uart), and the Interrupt Control and Status Register.

D TO A CONVERTERS

The four audio channels each have a DMA pointer register, data register, period, (frequency), register and volume register. Each channel has an on chip D to A (digital to analog) converter on the output. The four channels are grouped into a right and left audio output.

DISK CONTROL

The disk controller has registers for data read, data write and control. It also contains a Precompensation Output circuit, a Data separator input circuit with a digital phase lock loop.

UART CONTROL

The serial port uart included in Paula contains Data registers, Control registers, Transmit, (TRN), and receive registers.

POT CONTROL

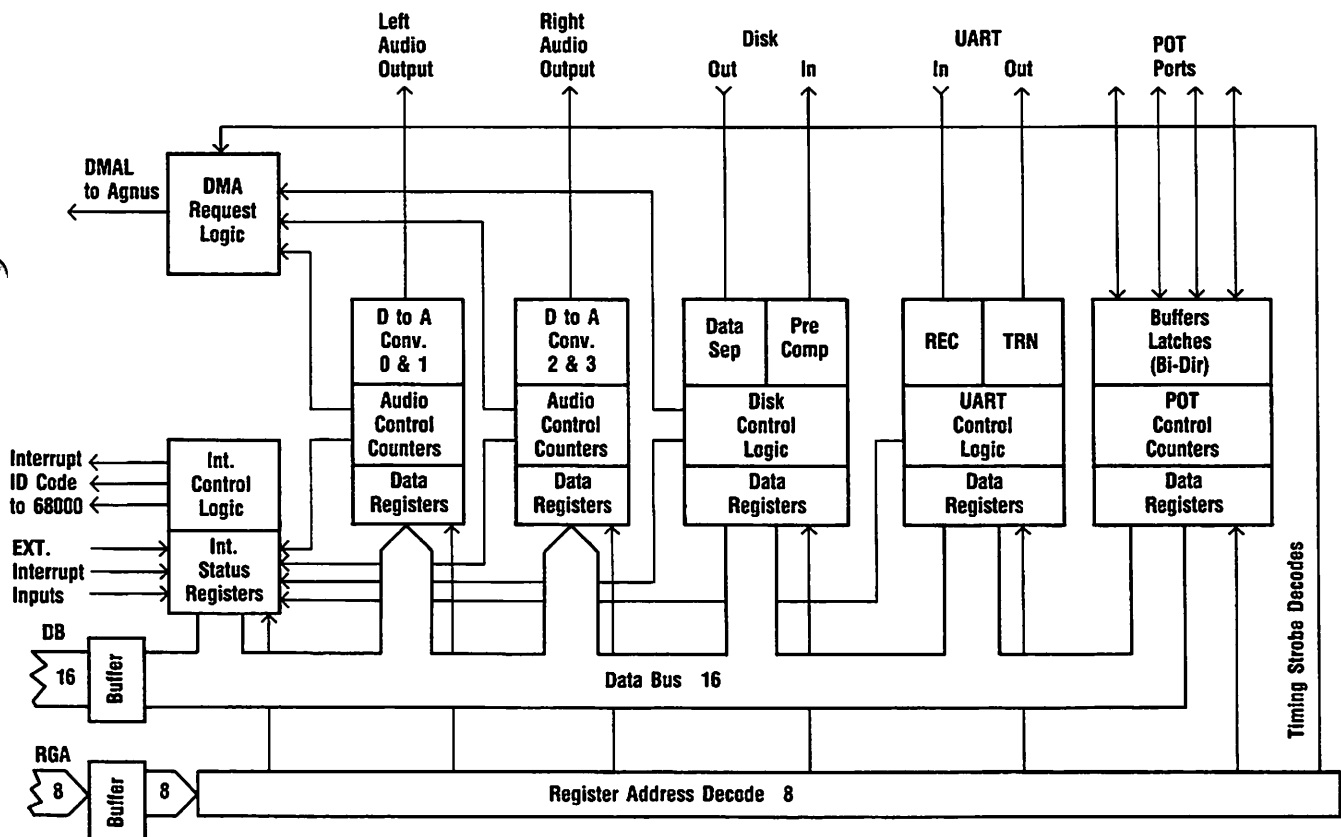
The four pot ports are general purpose I/O ports. They have counters for simple A to D (digital to analog) conversion of an external capacitor charging, which could also be used for analog joystick controllers.

INTERRUPT CONTROL

The audio, disk and uart controllers all set their own Interrupt Status register bits.

DMA REQUEST LOGIC

The audio and disk controllers also go to the DMA request logic, (remember: they are DMA users), causing the DMAL signal to request DMA cycles from Agnus.



Paula Block Diagram

GARY CUSTOM CONTROL CHIP

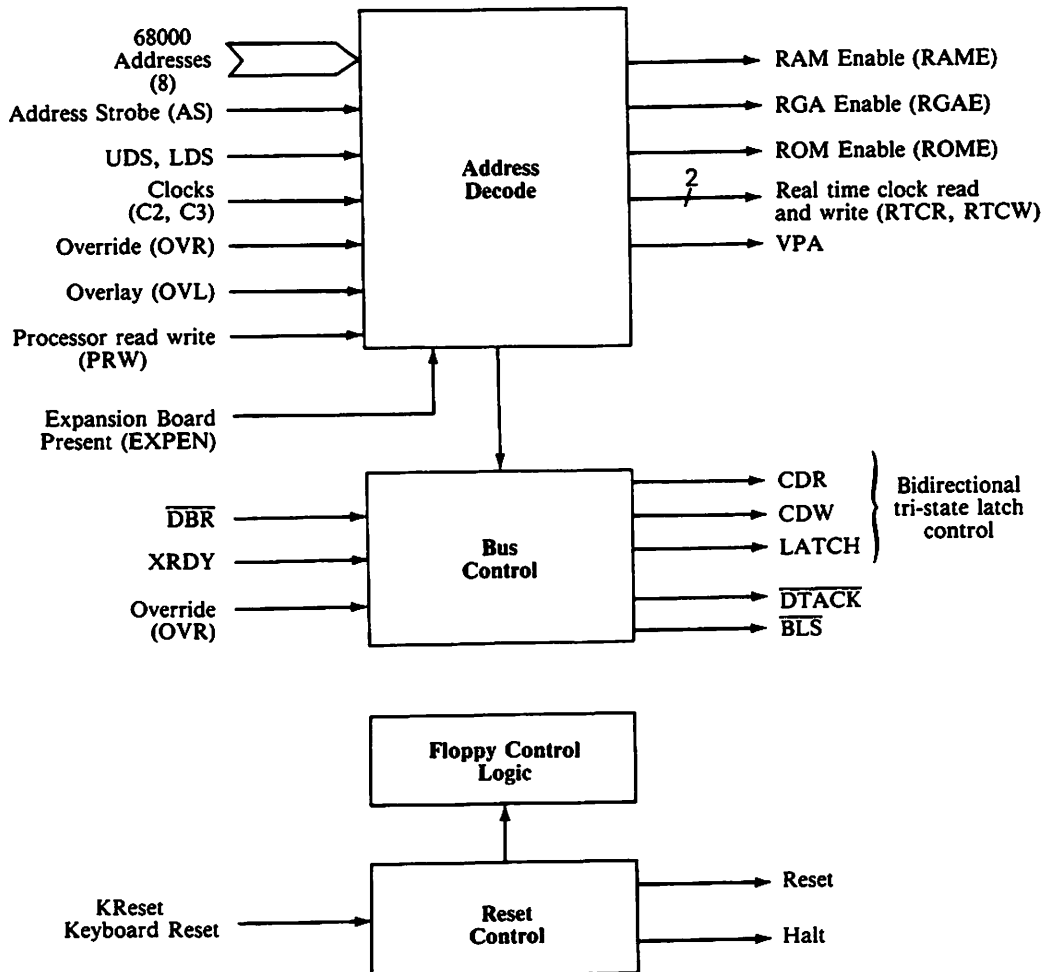
FEATURES

- Provides all bus control signals.
- Provides all address decoding.
- Generates the 68000 VPA signal.
- Handles some of the floppy circuitry.
- Provides keyboard reset interface.

For signal descriptions,
see Schematic #312813, sheet 1 of 10

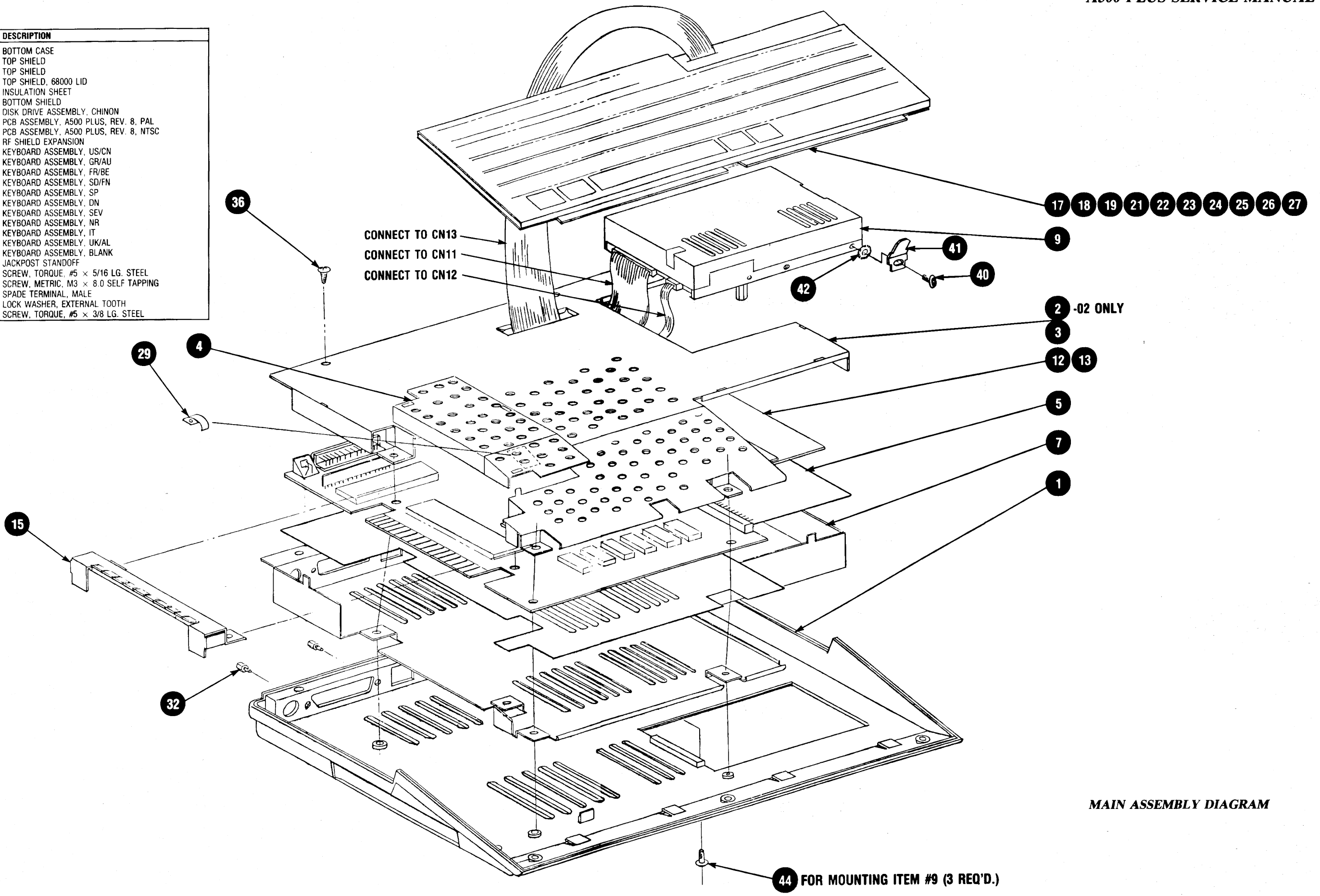
GND1	1	48	Vcc3
VPA	2	47	MTRX
DEL	3	46	MTRON
DEB	4	45	DKWDB
KBRESET	5	44	DKWEB
Vcc1	6	43	DTACK
MTR	7	42	HLT
DKWE	8	41	RST
DKWD	9	40	GND3
LDS	10	39	A23
UDS	11	38	A22
R/W	12	37	A21
AS	13	36	A20
BGACK	14	35	A19
BLIT	15	34	A18
SEL	16	33	A17
Vcc2	17	32	EXRAM
REGEN	18	31	XRDY
BLISS	19	30	OVL
RAMEN	20	29	OVR
ROMEN	21	28	CCK
CLKRD	22	27	CCKQ
CLKWR	23	26	CDAC
GND2	24	25	LATCH

GARY BLOCK DIAGRAM



SECTION 3
TROUBLESHOOTING

ITEM NO.	PART NO.	DESCRIPTION
1	312506-01	BOTTOM CASE
2	332358-01	TOP SHIELD
3	312504-02	TOP SHIELD
4	332359-01	TOP SHIELD, 68000 LID
5	312589-01	INSULATION SHEET
7	312590-01	BOTTOM SHIELD
9	312594-01	DISK DRIVE ASSEMBLY, CHINON
12	312812-01	PCB ASSEMBLY, A500 PLUS, REV. 8, PAL
13	312812-02	PCB ASSEMBLY, A500 PLUS, REV. 8, NTSC
15	327038-01	RF SHIELD EXPANSION
17	312502-01	KEYBOARD ASSEMBLY, US/CN
18	312502-02	KEYBOARD ASSEMBLY, GR/AU
19	312502-03	KEYBOARD ASSEMBLY, FR/BE
20	312502-05	KEYBOARD ASSEMBLY, SD/FN
21	312502-06	KEYBOARD ASSEMBLY, SP
22	312502-07	KEYBOARD ASSEMBLY, DN
23	312502-08	KEYBOARD ASSEMBLY, SEV
24	312502-09	KEYBOARD ASSEMBLY, NR
25	312502-04	KEYBOARD ASSEMBLY, IT
26	312502-12	KEYBOARD ASSEMBLY, UK/AL
27	312504-99	KEYBOARD ASSEMBLY, BLANK
32	390251-01	JACKPOST STANDOFF
36	390146-01	SCREW, TORQUE, #5 x 5/16 LG. STEEL
40	906800-03	SCREW, METRIC, M3 x 8.0 SELF TAPPING
41	252177-01	SPADE TERMINAL, MALE
42	905650-11	LOCK WASHER, EXTERNAL TOOTH
44	390146-02	SCREW, TORQUE, #5 x 3/8 LG. STEEL



MAIN ASSEMBLY DIAGRAM